is master and the other is slave. Switching the master from one clock module to the other will not cause any phase discontinuities or momentary bit transitions on output clock signals because the master and slave clock are phase locked with regard to one another prior to and after switching. Switching from one clock to the other may be initiated upon detection of a malfunction as indicated by an out-of-lock signal.

If there is a failure on the master clock module in US4282493, the signal from the slave unit will seamlessly take over. However, when the slave module takes over as master, the signal from this board is physically driven through the board of the previous master. If the previous master board is removed, all boards of the system will loose their clock signal; i.e. hot-swapping of the clock modules is not possible.

Moreover, apart from the PLL devices used for phase locking of the two sources, US4282493 assumes a PLL in the receiver end and requires additional logic on all boards of the system sharing a common clock in the same manner as in US6194969.

Summary of the invention

It is a primary object of the invention to set forth a system, which provides a virtually seamless clock signal if a local clock or clock unit malfunctions or a clock unit is hot swapped and which does not require a superior system component to secure redundancy.

This object has been accomplished by the subject matter defined in the claims. ~~by claim 1.~~

It is moreover an object to set forth an extendable clock system, which is based on a single modular unit.

This object has been accomplished by the subject matter defined in the claims. ~~by claim 2.~~

It is a further object of the invention to set forth a unit which provides a virtually seamless clock signal if a local clock or clock unit malfunctions or a clock unit is hot swapped and which does not require a superior system component to secure redundancy.

This object has been accomplished by the subject matter set forth in the claims. ~~in claim 8.~~